IDC-C1,AMD

~~Claim 9 line 1~~ 1-2 ~~delete "computer program product" and replace it with~~ -- computer-readable medium having encoded thereon computer-executable instructions --.

~~Claim 9, line 4, delete "computer program product including" and delete " for"~~ ✓ IDC-C2,AMD

~~Claim 12, line 1 delete, "computer program product" and replace it with~~ -- computer readable medium --.

7. The following is an examiner's statement of reasons for allowance:

While US Patent 6,223,142 teaches (claims 1 and 5) a computer-aided design and verification system a method for facilitating signal override in a simulation model of a digital circuit design that includes one or more design entities described utilizing a hardware description language (HDL), said method comprising: instantiating an instrumentation entity within at least one of said one or more design entities using port mapping fields designated by a non-conventional HDL comment syntax, said non-conventional HDL comment processed by a post-complier model build process, wherein said non-conventional HDL comment syntax is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including: a port name field; Wu et al., ("Digital PWM Control: Application in Voltage Regulation Modules") teaches (claims 1, 5 and 9) a post-compile model build process an input port map field containing data representing an input port at which said instrumentation entity receives a designated signal to be overridden and an output port mapping field comprising an override signal field specifying the name of said override signal, specifying the name of the port from